PATENT APPLICATION TRANSMITTAL LETTER
(Large Entity)

Docket No.
EN9-99-080

TO THE ASSISTANT COMMISSIONER FOR PATENTS

Transmitted herewith for filing under 35 U.S.C. 111 and 37 C.F.R. 1.53 is the patent application of:

Caletka et al.

For: **PARTIALLY CAPTURED ORIENTED INTERCONNECTIONS FOR BGA PACKAGES AND A METHOD OF FORMING THE INTERCONNECTIONS**

Enclosed are:

- ☒ Certificate of Mailing with Express Mail Mailing Label No. **EL396831592US**
- ☒ **Ten (10)** formal sheets of drawings.
- ☐ A certified copy of a application.
- ☒ Declaration ☒ Signed. ☐ Unsigned.
- ☒ Power of Attorney
- ☒ Information Disclosure Statement
- ☐ Preliminary Amendment
- ☒ Other: **Assignment and Assignment Cover Sheet**

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	26	- 20 =	6	x	$18.00	$108.00
Indep. Claims	5	- 3 =	2	x	$78.00	$156.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$760.00
					TOTAL FILING FEE	$1,024.00

- ☐ A check in the amount of to cover the filing fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **09-0457 (IBM)** as described below. A duplicate copy of this sheet is enclosed.
  - ☒ Charge the amount of **$1,024.00** as filing fee.
  - ☒ Credit any overpayment.
  - ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
  - ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Dated: Nov. 09, 1999

Signature

Lawrence R. Fraley, Esq.
Reg. No. 26,885
IBM Corporation
IP Law Dept. N50/040-4
1701 North Street
Endicott, NY 13760-5553
(607) 755-3207

cc:

Docket No. EN999080

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Caletka et al.

Serial No.: Group Art Unit:

Filed: herewith Examiner:

For: PARTIALLY CAPTURED ORIENTED INTERCONNECTIONS FOR BGA PACKAGES AND A METHOD OF FORMING THE INTERCONNECTIONS

Assistant Commissioner For Patents
Washington, D.C. 20231

EXPRESS MAIL CERTIFICATE

"Express Mail" label number: EL396831592US

Date of Deposit: 11/10/99

I hereby certify that the following **attached** paper or fee

Patent Application Fee Transmittal
Application
Drawings, 10 sheets, formal
Declaration, 3 pgs. (executed)
IDS, PTO-1449 & refs.
Assignment, 1 pg. (executed)
Recordation Form Cover Sheet
Postcard
Express Mail Cert.

is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner For Patents, Washington, D.C. 20231.

June M. Mitchell
(Name of person mailing paper or fee)

June M. Mitchell
(Signature of person mailing paper or fee)

NOTE: Each paper must have its own certificate and the "Express Mail" label number as a part thereof or attached thereto. When, as here, the certification is presented on a separate sheet, that sheet must (1) be signed and (2) fully identify and be securely attached to the paper or fee it accompanies. Identification should include the serial number and filing date of the application as well as the type of paper being filed, e.g., complete application, specification and drawings, responses to rejection or refusal, notice of appeal, etc. If the serial number of the application is not known, the identification should include at least the name of the inventor(s) and the title of the invention.

NOTE: The label number need not be placed on each page. It should, however, be placed on the first page of each separate document, such as, a new application, amendment, assignment, and transmittal letter for a fee, along with the certificate of mailing by "Express Mail". Although the label number may be on checks, such a practice is not required. In order not to deface formal drawings, it is suggested that the label number be placed on the back of each formal drawing or the drawings be accompanied by a set of informal drawings on which the label number is placed.

APPLICATION

FOR

UNITED STATES LETTERS PATENT

APPLICANT NAME: Caletka *et al.*

TITLE: PARTIALLY CAPTURED ORIENTED INTERCONNECTIONS FOR BGA PACKAGES AND A METHOD OF FORMING THE INTERCONNECTIONS

DOCKET NO. EN9-99-080

INTERNATIONAL BUSINESS MACHINES CORPORATION

CERTIFICATE OF MAILING UNDER 37 CFR 1.10

I hereby certify that, on the date shown below, this correspondence is being deposited with the United States Postal Service in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C., 20231 as "Express Mail Post Office to Addressee" Mailing Label No. EL396831592US

on 11/10/99

June M. Mitchell
Name of person mailing paper

June M. Mitchell 11/10/99
Signature Date

PARTIALLY CAPTURED ORIENTED INTERCONNECTIONS FOR BGA PACKAGES AND A METHOD OF FORMING THE INTERCONNECTIONS

BACKGROUND OF THE INVENTION

Technical Field

The present invention relates generally to Ball Grid Array (hereinafter "BGA") packages. In particular, the present invention relates to the use of partially captured interconnections, wherein the uncaptured region is selectively oriented in the direction of the highest stress within the BGA package.

Related Art

In the manufacture of BGA packages, thermal mismatch between the chip module and the printed circuit board may produce fatigue failure of the BGA interconnections, or solder joints. One solution for this problem is the elongation of the solder joints, which increases the compliance of the solder joints, thereby increasing the fatigue life of the BGA package. Solder joints have been elongated by the use of "captured pads" which form mask-defined solder joints. Along with increasing the height of the solder joint, the use of captured pads enhances the adhesion of the pads to the underlying chip module or printed circuit board. Unfortunately, stress concentrations within mask-defined

solder joints tends to decrease the fatigue life of the solder joints. Alternative techniques employed to elongate the solder joints and increase fatigue life include the use of spacers, high-melt solder columns, selective solder joints containing an excess solder volume, etc. However, many of these techniques reduce the amount of space on the printed circuit board available for wiring.

Accordingly, there exists a need in the industry for a BGA package having an increased fatigue life, without sacrificing wiring space.

SUMMARY OF THE INVENTION

The present invention provides an integrated chip package, e.g., a BGA package, having an increased fatigue life, enhanced pad adhesion, while maintaining sufficient wiring space. In particular, the present invention provides a method of forming an integrated chip package having solder joints that are mask-defined in a first direction and pad-defined in a second direction.

The first general aspect of the present invention provides a method of forming an integrated chip package, comprising the steps of: providing a first substrate and a second substrate, each having conductive pads thereon; applying a mask to at least one of the first and second substrates, wherein the mask has a

plurality of non-circular openings having a first dimension and a second dimension, such that the conductive pads are not covered by the mask in the direction of the first dimension and partially covered by the mask in the direction of the second dimension; and providing a reflowable material between the conductive pads of the first and second substrates. This aspect allows for an integrated chip package, e.g., a BGA package, having an increased fatigue life, without sacrificing wiring space. It also allows for an integrated chip package having solder joints that are mask-defined in a first direction and pad-defined in a second direction.

The second aspect of the present invention provides an integrated chip package comprising: a first substrate and a second substrate, wherein at least one of the first and second substrates includes a plurality of partially captured pads; and a plurality of interconnections between the first and second substrates. This aspect provides similar advantages as those associated with the first aspect.

The third aspect of the present invention provides a substrate having a plurality of conductive pads and a mask thereon, wherein the mask has a plurality of openings having a first dimension larger than the conductive pad, and a second dimension smaller than the conductive pad. This aspect provides similar advantages as those associated with the first aspect.

The fourth aspect of the present invention provides an integrated circuit mask having a plurality of elongated non-circular openings therein, wherein the openings have a first dimension greater than a second dimension, such that the first dimension of the openings coincides with the direction of the highest stress within integrated circuit. This aspect provides similar advantages as those associated with the first aspect.

The fifth aspect of the present invention provides an integrated circuit interconnection, wherein the interconnection is mask-defined in a first direction and pad-defined in a second direction. This aspect provides similar advantages as those mentioned with respect to the first aspect.

The foregoing and other features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The preferred embodiments of this invention will be described in detail, with reference to the following figures, wherein like designations denote like elements, and wherein:

Fig. 1 depicts a cross-sectional view of a semiconductor chip module (having a mask removed for clarity) in accordance with a preferred embodiment of the present invention;

Fig. 2 depicts a cross-sectional view of a printed circuit

board (having a mask removed for clarity) in accordance with a preferred embodiment of the present invention;

Fig. 3 depicts a bottom view of the semiconductor chip module having a mask thereon in accordance with a preferred embodiment of the present invention;

Fig. 4 depicts a top view of the printed circuit board having a mask thereon in accordance with a preferred embodiment of the present invention;

Fig. 5 depicts an enlarged view of an opening within the mask covering the semiconductor chip module and/or the printed circuit board in accordance with a preferred embodiment of the present invention;

Fig. 6 depicts a cross-sectional view of the semiconductor chip module, with the mask removed for clarity, having solder balls attached thereto in accordance with a preferred embodiment of the present invention;

Fig. 7 depicts a cross-sectional view of an integrated chip package, with the mask removed for clarity, in accordance with a preferred embodiment of the present invention;

Fig. 8 depicts a cross-sectional view of a solder joint along the major axis of the mask opening, with the mask removed for clarity, in accordance with a preferred embodiment of the present invention;

Fig. 9 depicts a cross-sectional view of a solder joint

along the minor axis of the mask opening in accordance with a preferred embodiment of the present invention;

Fig. 10 depicts a top view of related art mask openings having a plurality of wires are mounted therebetween; and

Fig. 11 depicts a top view of elongated mask openings having a plurality of wires mounted therebetween in accordance with a preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Although certain preferred embodiments of the present invention will be shown and described in detail, it should be understood that various changes and modifications may be made without departing from the scope of the appended claims. The scope of the present invention will in no way be limited to the number of constituting components, the materials thereof, the shapes thereof, the relative arrangement thereof, etc., and are disclosed simply as an example of the preferred embodiment. Although the drawings are intended to illustrate the present invention, the drawings are not necessarily drawn to scale.

Referring to the drawings, Fig. 1 shows a semiconductor chip module 10 having an integrated circuit chip 12 electrically and mechanically connected to a first surface 13 of a chip carrier 14. The chip carrier 14 is made of an insulative non-wettable material, such as ceramic, FR4, IBM's Dry-Clad™, LCP (Liquid

Crystal Polymer) polyimide, etc. A plurality of circular conductive pads 16 are mounted on a second surface 18 of the chip carrier 14, using a process well known in the industry. The conductive pads 16 are preferably made of copper, or some other suitable material known and used in the art.

Fig. 2 shows a printed circuit card or board 20 upon which the module 10 will be mounted. The board 20 is made of an insulative non-wettable material, i.e., ceramic, FR4, IBM's Dry-Clad™, LCP (Liquid Crystal Polymer) polyimide, etc. A plurality of circular conductive pads 22 are affixed to a first surface 24 of the board 20. The conductive pads 22 are preferably copper, and coincide with the location of the conductive pads 16 on the chip carrier 14 of the module 10.

Fig. 3 shows the second surface 18 of the chip carrier 14 (refer to Fig. 1) covered with a mask 26. Similarly, Fig. 4 shows the first surface 24 of the board 20 covered with a mask 28. The masks 26, 28 have elongated non-circular, oblong, oval, or elliptical openings 30 located over the conductive pads 16, 22. As illustrated in Fig. 5, the elongated openings 30 within the masks 26, 28 covering the conductive pads 16, 22, respectively, have a major axis 32 and a minor axis 34. The major axis 32 has a dimension 36 that is greater than the diameter 38 of the conductive pads 16, 22. The regions of the conductive pads 16, 22 proximate the major axis 32 of the

conductive pads 16, 22 are exposed or "un-captured" by the masks 26, 28. In contrast, the minor axis 34 has a dimension 40 that is less than the diameter 42 of the conductive pads 16, 22. In regions 44, the conductive pads 16, 22 are partially covered or "captured" by the masks 26, 28.

Fig. 6 shows a plurality of solder balls 47, having the mask 26 removed for clarity, attached or "wetted" to the exposed or un-captured regions of the conductive pads 16, using methods known in the industry. Specifically, the solder balls 47 wet to the regions of the conductive pads 16 that are not covered by the masks 26. The module 10, having solder balls 47 attached thereto, is then mounted to the board 20. In particular, the free ends 49 of the solder balls 47 wet to the exposed or un-captured regions of the conductive pads 22 of the board 20, using methods well known in the art. Fig. 7 shows a cross-sectional view of an integrated chip package 46, in this example a BGA package, having the masks 26, 28 removed for clarity, produced after the module 10 and the board 20 are connected by a plurality of solder joints 48.

Fig. 8 shows a cross-sectional view of a solder joint 48, having the mask 28 removed for clarity, taken along the major axis 32 of the openings 30 (refer to Fig. 5). In particular, the conductive pads 16, 22 of the module 10 and the board 20, respectively, are un-captured along the major axis 32. The

wettable area (the area to which the solder balls adhere) of the conductive pads 16, 22 along the major axis 32 is equal to the diameter 38 of the conductive pads 16. Therefore, the solder balls 47 wet to the entire diameter 38 of the conductive pads 16, 22 forming un-captured or pad-defined solder joints in the direction of the major axis 32. The solder balls 47 do not wet to the surrounding surfaces 18, 24 of the chip carrier 14 and the board 20 because the chip carrier 14 and the board 20 are made of non-wettable materials.

Fig. 9 shows a cross-sectional view of a solder joint 48 taken along the minor axis 34 of the openings 30 (refer to Fig. 5). The conductive pads 16, 22 of the module 10 and the board 20 are partially captured by the masks 26, 28 (see regions 44 shown in Fig. 5). Therefore, the wettable area of the conductive pads 16, 22 along the minor axis 34 is equal to the dimension 40 of the openings 30 in the masks 26, 28 in the direction of the minor axis 34, rather than the diameter 42 of the conductive pads 16, 22 (as in the direction of the major axis 32). As a result, the solder balls 47 wet only to the area of the conductive pads 16, 22 exposed by the openings 30 in the masks 26, 28 forming captured or mask-defined solder joints in the direction of the minor axis 34.

The major axis 32 of the elongated openings 30 is preferably selectively oriented in the direction of greatest

stresses, predominantly shear stresses, within the solder joints 48 attached to the chip carrier 14 and the board 20. However, the major axis 32 of the elongated openings 30 may be oriented in any number of directions as needed or desired. Figs. 3 and 4 depict a possible orientation that may be used, particularly for a square chip carrier 14 and board 20, wherein the stresses generally extend radially from a center 60, 61 of the chip carrier 14 and the board 20, respectively. The mask-defined solder joint profile taken along the minor axis 34, illustrated in Fig. 9, shows a plurality of discontinuities 50 within the solder joint 48, where the mid-section 52 abruptly meets a restricted section 54. Stress concentrations are present at the discontinuities 50 which tend to reduce the fatigue life of mask-defined solder joints if significant stress is applied to these regions. However, the profile of the pad-defined solder joint taken along the major axis 32, illustrated in Fig. 8, shows that no such discontinuities 50 are present within the high stress region.

The use of a solder joint 48 utilizing a combination of mask-defined and pad-defined solder joint profiles (see Figs. 8 and 9) provides several advantages. For example, the mask-defined solder joints have a higher equilibrium height than pad-defined solder joints. Again, this is desirable because elongated solder joints tend to be more compliant, therefore less

likely to fracture or break. Equilibrium height is the normal height reached by the solder joint as the internal pressure of the molten solder joint equals the weight that it supports. This is attributable to the restricted sections 54 of mask-defined solder joints (illustrated in Fig. 9), which tend to lengthen or elongate the solder joints 48. Further, mask-defined solder joints tend to have enhanced adhesion strength. Adhesion strength is the ability of the conductive pad to remain attached to the underlying substrate. In this case, the mask-defined solder joints (Fig. 9) enhance the adhesion strength of the conductive pads 16, 22 to the chip carrier 14 and the board 20, namely in regions 44 (refer to Fig. 5) where the masks 26, 28 cover the conductive pads 16, 22. These attributes are combined with pad-defined solder joints (illustrated in Fig. 8), which eliminate the internal stress concentrations found at the discontinuities 50 of the mask-defined solder joints (shown in Fig. 9). Therefore, using a mask having openings that form solder joints that are a combination of both pad-defined and mask-defined solder joints increases the fatigue life of the solder joints 48.

It should be noted that use of elongated openings 30, rather than round mask openings, also increases the space available for wiring. The major axis 32 of the openings 30 in the masks 26, 28 should be oriented in the direction of highest stress, taking

into consideration the orientation that maximizes the space on the board 20 available for wiring. Fig. 10 shows the limited amount of space available for wiring when related art circular mask openings 162 are used with elliptical pads. Only three traces or wires 164 fit between the circular mask openings 162. In contrast, Fig. 11 shows the increased space available when elongated openings 30 are used in accordance with the preferred embodiment of the present invention. At least four traces or wires 66 fit between the elongated mask openings 30.

It should be understood that the oval-shaped elongated openings 30, oriented radially from the centers 60, 61 of the chip carrier 14 and the board 20, are solely an example. The elongated openings 30 are not limited to the size, shape or orientation described and illustrated herein. Likewise, the size and shape of the conductive pads 16, 22 are not limited by the disclosure above. A vast array of size, shape and orientation combinations may be used to suit particular needs.

It should also be noted that the mask does not have to be applied to both the chip carrier 14 and the board 20, as described above. Rather, the mask may be used on only one side of the BGA package, either the chip carrier 14 or the board 20. This would produce solder joints having the combination pad-defined and mask-defined solder joint profile, described and illustrated above, at one end of the solder joint and an

alternative profile at the other end. For instance, the other end may have a solder joint profile that is entirely pad-defined or entirely mask-defined, etc.

While this invention has been described in conjunction with the specific embodiments outlined above, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art. Accordingly, the preferred embodiments of the invention as set forth above are intended to be illustrative, not limiting. Various changes may be made without departing from the spirit and scope of the invention as defined in the following claims.

CLAIMS

We claim:

1. A method of forming an integrated chip package, comprising the steps of:

providing a first substrate and a second substrate, each having conductive pads thereon;

applying a mask to at least one of the first and second substrates, wherein the mask has a plurality of non-circular openings having a first dimension and a second dimension, such that the conductive pads are not covered by the mask in the direction of the first dimension and partially covered by the mask in the direction of the second dimension; and

providing a reflowable material between the conductive pads of the first and second substrates.

2. The method of claim 1, wherein the first dimension of the elongated non-circular openings is greater than the second dimension of the non-circular openings.

3. The method of claim 1, wherein the first dimension of the non-circular openings is selectively oriented in the direction of highest stress for each interconnection formed from the reflowable material within the integrated chip package.

4. The method of claim 1, wherein the non-circular openings of the mask are elliptical.

5. The method of claim 1, wherein the conductive pads are circular.

6. The method of claim 5, wherein the conductive pads are copper.

7. The method of claim 1, wherein the mask comprises a non-wettable material.

8. The method of claim 7, wherein the mask comprises an epoxy.

9. The method of claim 1, wherein the first substrate is a chip carrier.

10. The method of claim 1, wherein the second substrate is a printed circuit board.

11. The method of claim 1, wherein the reflowable material is solder.

12. The method of claim 1, wherein a plurality of traces are mounted between the non-circular openings of the mask.

13. The method of claim 1, wherein the integrated chip package is a Ball Grid Array package.

14. An integrated chip package comprising:

a first substrate and a second substrate, wherein at least one of the first and second substrates includes a plurality of partially captured pads; and

a plurality of interconnections between the first and second substrates.

15. The integrated chip package of claim 14, wherein the plurality of partially captured pads are formed by a mask having elongated non-circular mask openings.

16. The integrated chip package of claim 15, wherein the elongated non-circular mask openings have a first dimension and a second dimension.

17. The integrated chip package of claim 16, wherein the first dimension of the elongated non-circular mask openings is greater than the second dimension of the elongated non-circular mask openings.

18. The integrated chip package of claim 16, wherein the first dimension of the elongated non-circular mask openings is selectively oriented on the substrate in the direction of highest stress within each interconnection.

19. The integrated chip package of claim 14, wherein the interconnections have a combination of mask-defined and pad-defined solder joint profiles.

20. A substrate having a plurality of conductive pads and a mask thereon, wherein the mask has a plurality of openings having a first dimension larger than the conductive pad, and a second dimension smaller than the conductive pad.

21. The substrate of claim 20, wherein the conductive pads are circular.

22. The substrate of claim 20, wherein the first dimension of the openings is greater than the second dimension of the openings.

23. The substrate of claim 22, wherein the first dimension of the openings is selectively oriented in the direction of highest stress within a plurality of interconnections formed within the openings of the substrate.

24. An integrated circuit mask having a plurality of elongated non-circular openings therein, wherein the openings have a first dimension greater than a second dimension, such that the first dimension of the openings coincides with the direction of the highest stress within the integrated circuit.

25. The integrated circuit mask of claim 24, wherein the mask comprises a non-wettable material.

26. An integrated circuit interconnection, wherein the interconnection is mask-defined in a first direction and pad-defined in a second direction.

PARTIALLY CAPTURED ORIENTED INTERCONNECTIONS FOR BGA PACKAGES AND A METHOD OF FORMING THE INTERCONNECTIONS

ABSTRACT OF THE DISCLOSURE

A Ball Grid Array package having an increased fatigue life and improved conductive pad adhesion strength, as well as providing sufficient wiring space within the package, is disclosed. In particular, solder joints having a combination of mask-defined and pad-defined solder joint profiles are formed using a mask having non-circular elongated openings. The non-circular elongated openings of the mask have a major axis and a minor axis, such that the dimension of the openings along the major axis is greater than the diameter of the conductive pads, and the dimension of the openings along the minor axis is less than the diameter of the conductive pads. In addition, the major axis of the openings within the mask are selectively oriented in the direction of highest stress for each solder joint within the package, while providing ample wiring space therein.

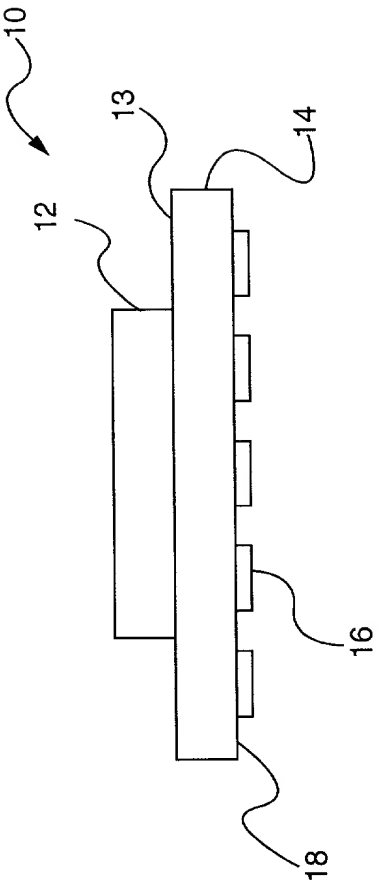

FIG. 1

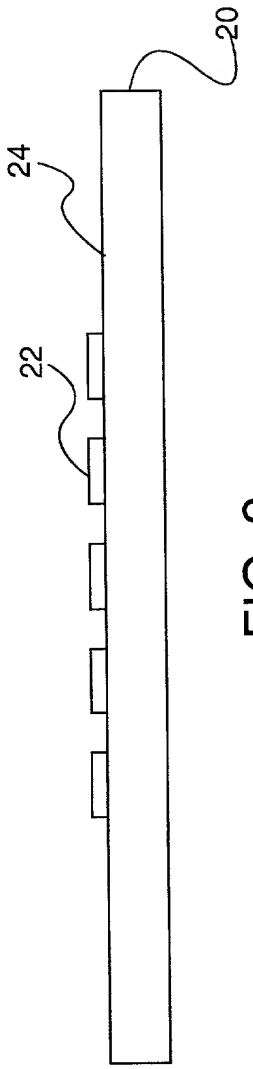

FIG. 2

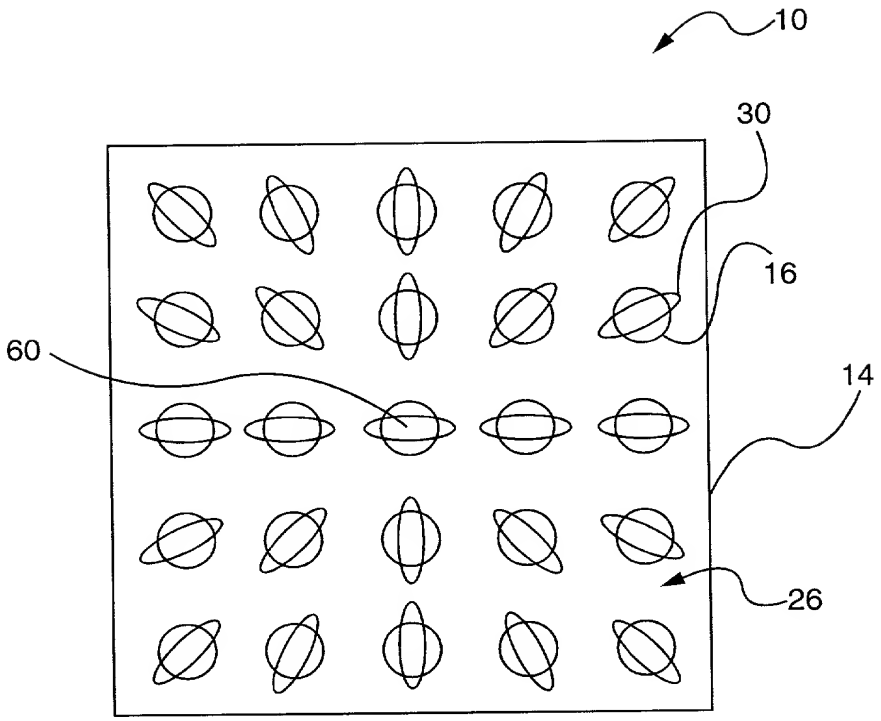

FIG. 3

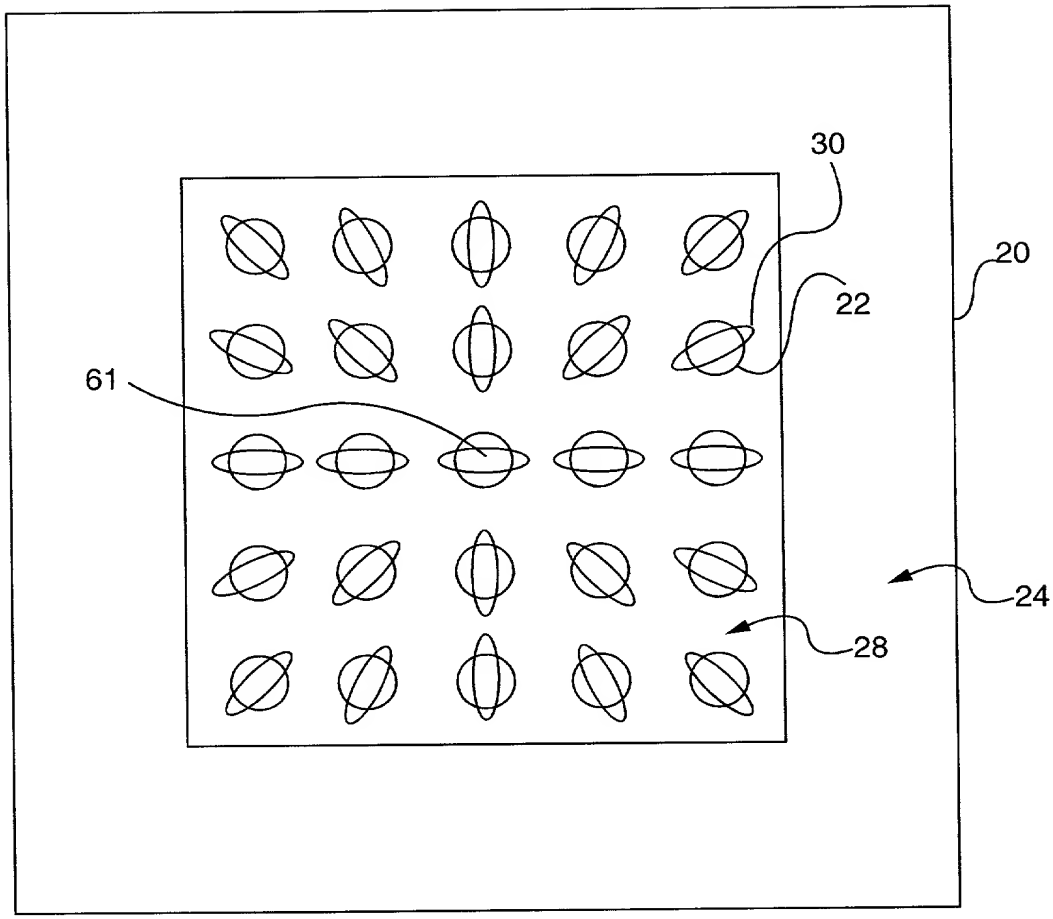

FIG. 4

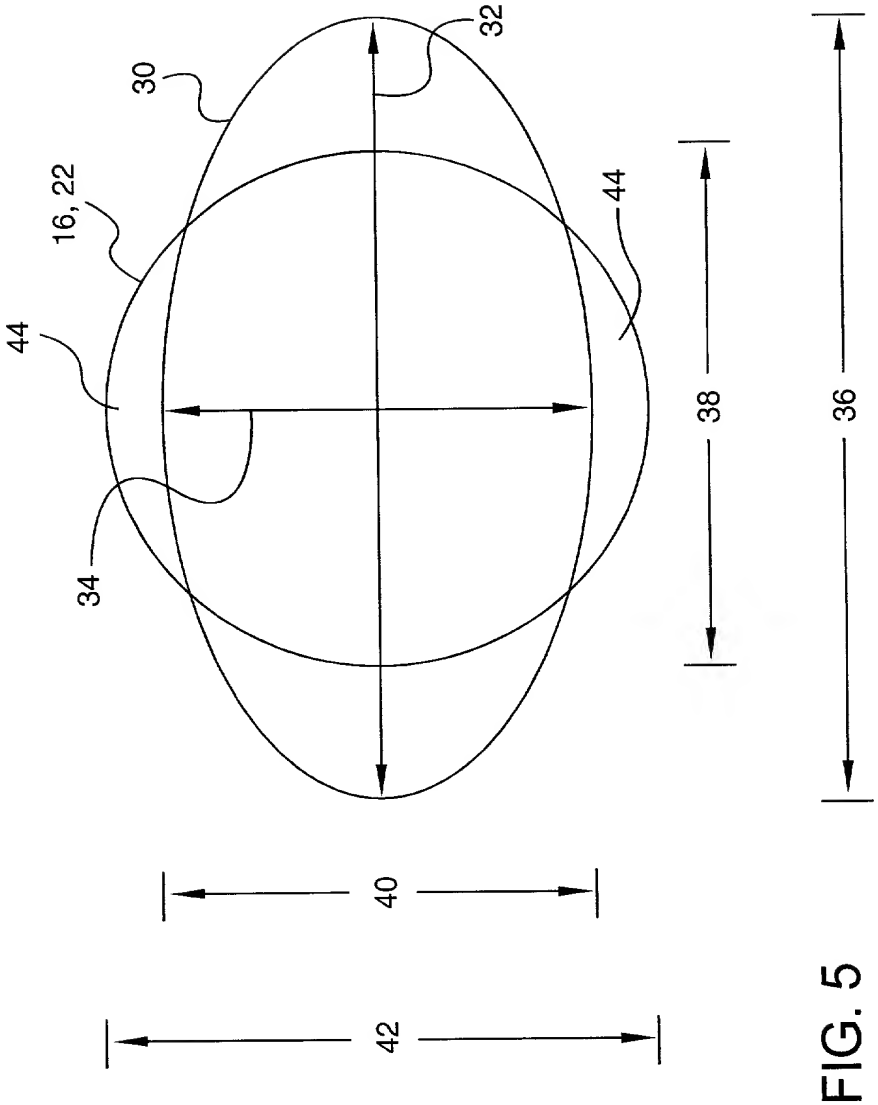

FIG. 5

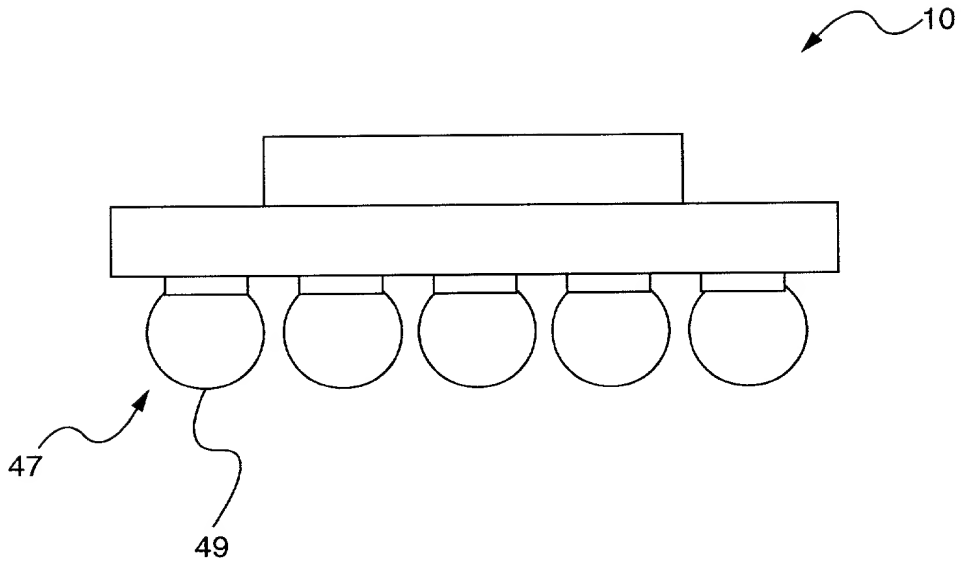

FIG. 6

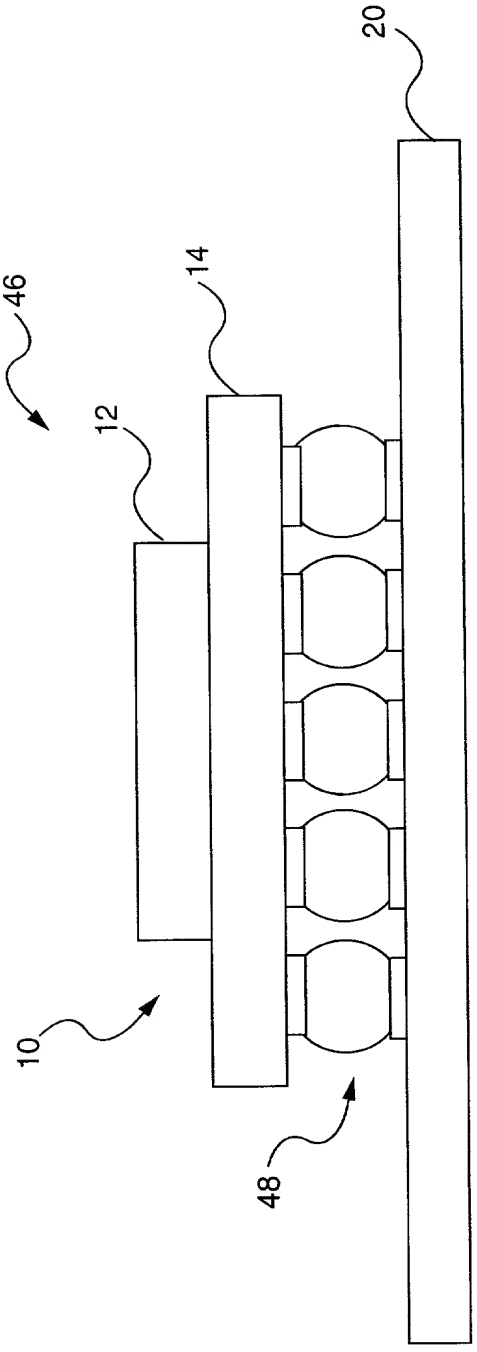

FIG. 7

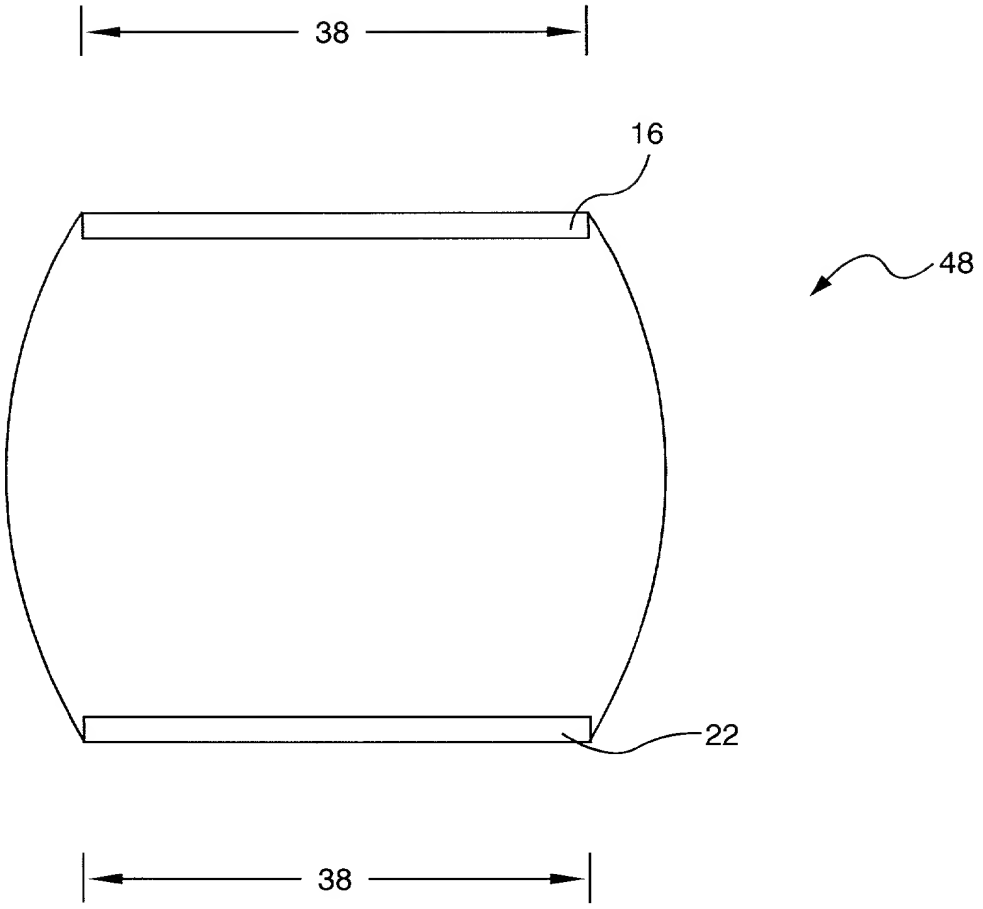

FIG. 8

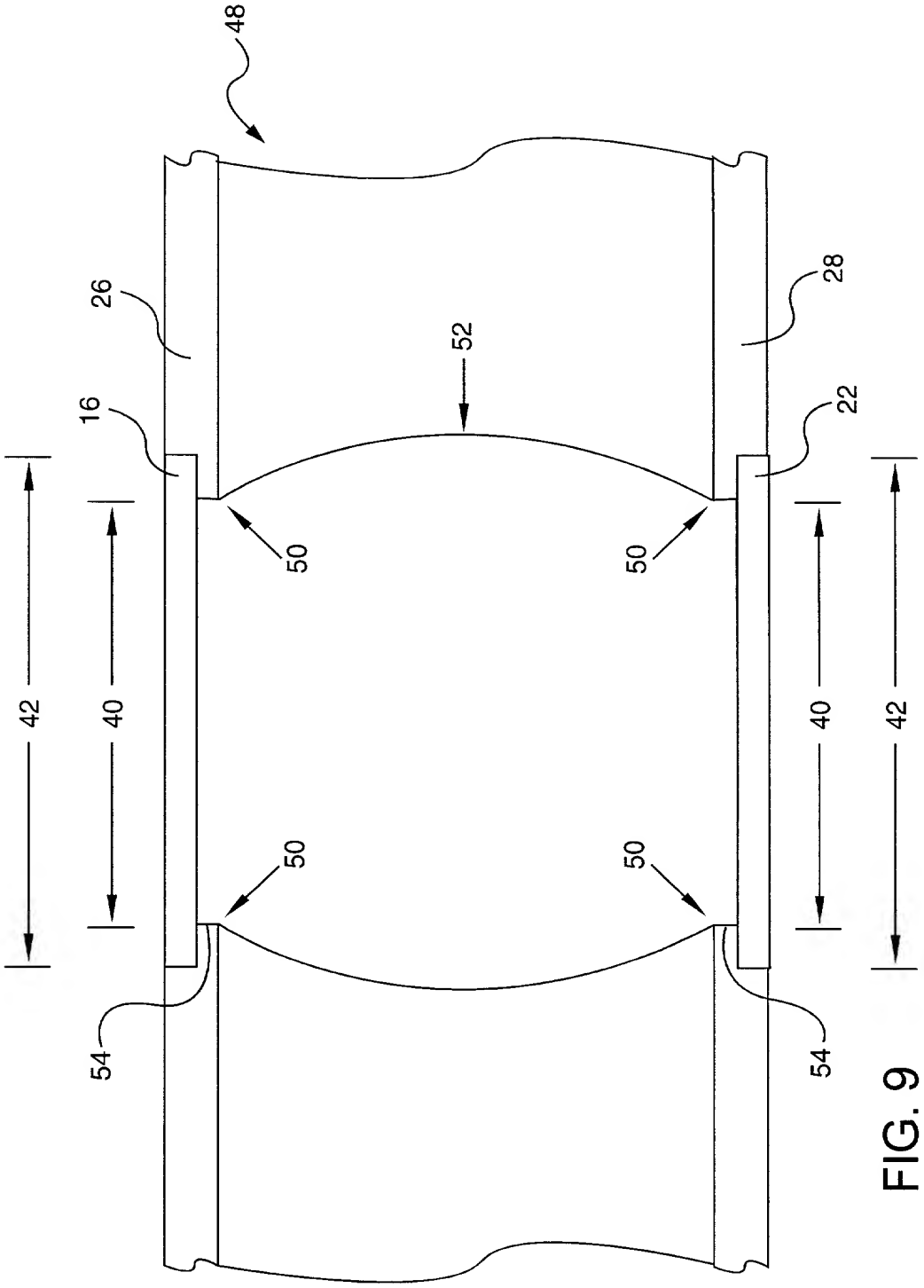

FIG. 9

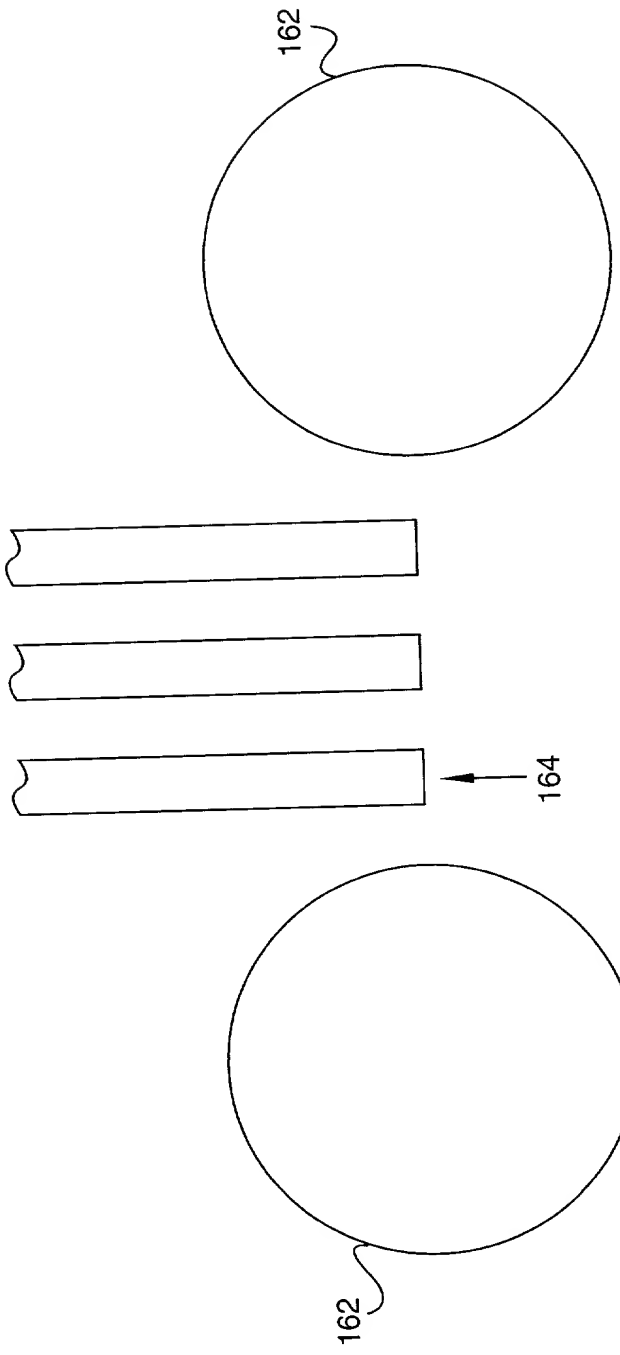

FIG. 10 (RELATED ART)

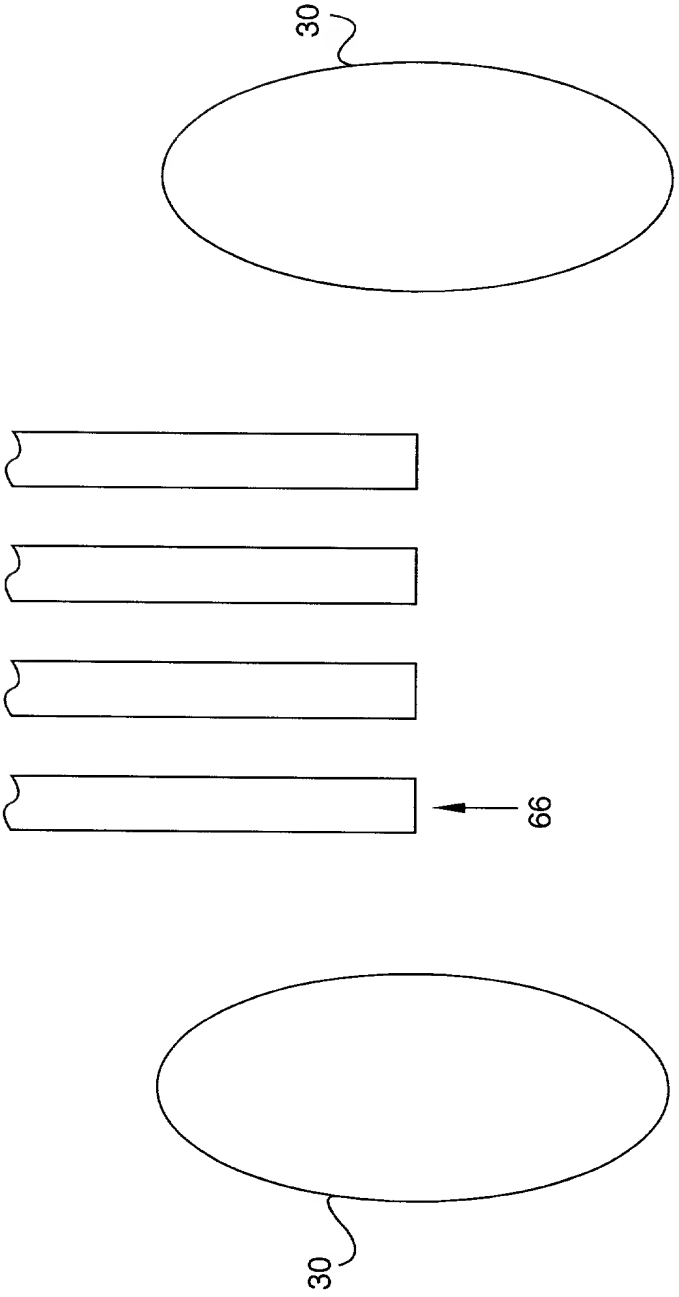

FIG. 11

Docket No.
EN9-99-080

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

PARTIALLY CAPTURED ORIENTED INTERCONNECTIONS FOR BGA PACKAGES AND A METHOD OF FORMING THE INTERCONNECTIONS

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on _____ as United States Application No. or PCT International Application Number _____

and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐

EN9-99-080

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

en9-99-080

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

Albert L. Schmeiser - 30,681
Arlen L. Olsen - 37,543
John A. Merecki - 35,812
S. Jared Pitts -38,579
Kristen L. Humiston - Ashdown - 43,682
Jack P. Friedman - 44,688
Robert J. Mauri - 41,180
Lori J. Howland - 42,671
Ziye Zhou - 41,423
David L. Adour - 29,604
Lawrence R. Fraley - 26,885
William H. Steinberg - 28,540
Arthur J. Samodovitz - 31,297
Christopher A. Hughes - 26,914
Edward A. Pennington - 32,588
John E. Hoel - 26,279
Joseph C. Redmond, Jr. - 18,753

Send Correspondence to: **Kristen L. Humiston-Ashdown**
Schmeiser, Olsen & Watts
3 Lear Jet Lane - Suite 201
Latham, N.Y. 12110

Direct Telephone Calls to: *(name and telephone number)*
Kristen L. Humiston (518) 220-1850

Full name of sole or first inventor
David V. Caletka

Sole or first inventor's signature — Date
11/5/99

Residence
428 Tobey Road, Apalachin, New York 13732

Citizenship
U.S.A.

Post Office Address
Same as Residence

Full name of second inventor, if any
Eric A. Johnson

Second inventor's signature — Date
11/5/99

Residence
7 Jeffrey Heights, Greene, New York 13778

Citizenship
U.S.A.

Post Office Address
Same as Residence